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////////////////////////////////////
////
//Project       : DXXX
//
//Organization: aaa
//
//Author        : abc
//
5 //Date         : 12-02-2008
//
////////////////////////////////////
////
//provided, it won't be asserted, which is ok as analog IO disabled outside APR.
10 module abc ();

    if( ((~SEL16 && sclk_cnt>= 5'd14) || (SEL16 && sclk_cnt>= 5'd22)) && ~
ft_flag) || (sclk_cnt>= 5'd30 && ft_flag))
        COUNT_OK <= 1'b1;
    end

15    always@(negedge PORB or posedge SCLKB)
        if( (~ft_flag && ((~SEL16 && sclk_cnt!=5'd15) || (SEL16 && sclk_cnt!=5'
d23))) || (ft_flag && sclk_cnt!=5'd31) )
            spi_sh_reg[31:0] <= {spi_sh_reg[30:0], DIN};
        end

20    always @(negedge rb_spi_done or posedge SCLKB)
        if(~rb_spi_done)
            SPI_DONE <= 1'b0;
        else if(~ft_flag && ((~SEL16 && sclk_cnt==5'd15) || (SEL16 && sclk_cnt==5'
d23)) )
25            SPI_DONE <= 1'b1;

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        always@(negedge PORB or posedge SCLKB)
            if( (~ft_flag && ((~SEL16 && sclk_cnt!=5'd15) || (SEL16 && sclk_cnt!=5'
d23))) || (ft_flag && sclk_cnt!=5'd31) )
                spi_sh_reg[31:0] <= {spi_sh_reg[30:0], DIN};
50        end

        always@(negedge PORB or posedge SCLKB)
55        if( (~ft_flag && ((~SEL16 && sclk_cnt!=5'd15) || (SEL16 && sclk_cnt!=5'
d23))) || (ft_flag && sclk_cnt!=5'd31) )
            spi_sh_reg[31:0] <= {spi_sh_reg[30:0], DIN};
        end

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60    always@(negedge PORB or posedge SCLKB)
        if( (~ft_flag && ((~SEL16 && sclk_cnt!=5'd15) || (SEL16 && sclk_cn
d23))) || (ft_flag && sclk_cnt!=5'd31) )
            spi_sh_reg[31:0] <= {spi_sh_reg[30:0], DIN};
        end
65

        always@(negedge PORB or posedge SCLKB)
            if( (~ft_flag && ((~SEL16 && sclk_cnt!=5'd15) || (SEL16 && sclk_cn
d23))) || (ft_flag && sclk_cnt!=5'd31) )
                spi_sh_reg[31:0] <= {spi_sh_reg[30:0], DIN};
70        end

        always@(negedge PORB or posedge SCLKB)
            if( (~ft_flag && ((~SEL16 && sclk_cnt!=5'd15) || (SEL16 && sclk_cn
d23))) || (ft_flag && sclk_cnt!=5'd31) )
75                spi_sh_reg[31:0] <= {spi_sh_reg[30:0], DIN};
        end

endmodule

```