```
////////////////////////////////////////////////////////////////////////////////
/////
//Project     : DXXX
   //
//Organization: aaa
   //
//Author      : abc
   //
//Date        : 12-02-2008
   //
////////////////////////////////////////////////////////////////////////////////
/////

//provided, it won't be asserted, which is ok as analog IO disabled outside APR.

module abc ();

         if( (((~SEL16 && sclk_cnt>= 5'd14) || (SEL16 && sclk_cnt>= 5'd22)) && ~
ft_flag) || (sclk_cnt>= 5'd30 && ft_flag))
            COUNT_OK <= 1'b1;
      end

   always@(negedge PORB or posedge SCLKB)
         if( (~ft_flag && ((~SEL16 && sclk_cnt!=5'd15) || (SEL16 && sclk_cnt!=5'
d23))) || (ft_flag && sclk_cnt!=5'd31) )
            spi_sh_reg[31:0] <= {spi_sh_reg[30:0], DIN};
      end

   always @(negedge rb_spi_done or posedge SCLKB)
      if(~rb_spi_done)
         SPI_DONE <= 1'b0;
      else if(~ft_flag && ((~SEL16 && sclk_cnt==5'd15) || (SEL16 && sclk_cnt==5'
d23)) )
         SPI_DONE <= 1'b1;













   always@(negedge PORB or posedge SCLKB)
         if( (~ft_flag && ((~SEL16 && sclk_cnt!=5'd15) || (SEL16 && sclk_cnt!=5'
d23))) || (ft_flag && sclk_cnt!=5'd31) )
            spi_sh_reg[31:0] <= {spi_sh_reg[30:0], DIN};
      end



   always@(negedge PORB or posedge SCLKB)
         if( (~ft_flag && ((~SEL16 && sclk_cnt!=5'd15) || (SEL16 && sclk_cnt!=5'
d23))) || (ft_flag && sclk_cnt!=5'd31) )
            spi_sh_reg[31:0] <= {spi_sh_reg[30:0], DIN};
      end
```



```


   always@(negedge PORB or posedge SCLKB)
         if( (~ft_flag && ((~SEL16 && sclk_cnt!=5'd15) || (SEL16 && sclk_cn
d23))) || (ft_flag && sclk_cnt!=5'd31) )
            spi_sh_reg[31:0] <= {spi_sh_reg[30:0], DIN};
      end


   always@(negedge PORB or posedge SCLKB)
         if( (~ft_flag && ((~SEL16 && sclk_cnt!=5'd15) || (SEL16 && sclk_cn
d23))) || (ft_flag && sclk_cnt!=5'd31) )
            spi_sh_reg[31:0] <= {spi_sh_reg[30:0], DIN};
      end


   always@(negedge PORB or posedge SCLKB)
         if( (~ft_flag && ((~SEL16 && sclk_cnt!=5'd15) || (SEL16 && sclk_cn
d23))) || (ft_flag && sclk_cnt!=5'd31) )
            spi_sh_reg[31:0] <= {spi_sh_reg[30:0], DIN};
      end

endmodule
```